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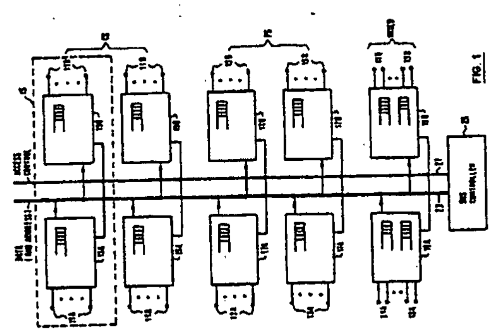
(54) Method and apparatus for switching information between channels for synchronous information traffic and asynchronous data packets.

(57) In a switching exchange for circuit-switched/synchronous traffic (CS) and packet-switched/asynchronous data packet traffic (PS), transmission lines (11 A, 11 B, 13 A, 13 B) communicate with FIFO buffers interconnected by a data bus (23) on which information is transferred in periodic frames. CS traffic is collected in FIFO input buffers in minipackets each carrying a local routing address. The last minipacket per frame period is identified by a special end tag. Once per frame a daisy-chain signal propagates through access control lines (27), to sequentially read out from FIFO input buffers all CS minipackets up to the next one having a special end tag, transferring them through the data bus to FIFO output buffers. Thereafter a token access mechanism starts enabling selective PS data packet transfer between FIFO input and output buffers. When a new frame begins, any PS data packet transfer in interrupted for a CS minipacket readout process, and thereafter transfer of the interrupted PS packet is resumed.



EP 0 276 349 A1

METHOD AND APPARATUS FOR SWITCHING INFORMATION BETWEEN CHANNELS FOR SYNCHRONOUS INFORMATION TRAFFIC AND ASYNCHRONOUS DATA PACKETS

FIELD OF INVENTION

Present invention relates to switching exchanges, in particular to a method for transferring information between channels carrying synchronous information traffic and channels carrying asynchronous data packet traffic, and to switching exchange apparatus for interconnecting communication lines carrying synchronous information traffic and communication lines carrying asynchronous data packets.

BACKGROUND

In communications, there is an increasing interest for the transmission of various kinds of information such as computer data and voice signals over the same network. This requires facilities for integrated services. Among these, switches or exchanges are important which can transfer streams of information or data bursts between various lines or channels which are connected to such exchanges or network nodes.

Various systems were designed which can handle the different kinds of traffic in an integrated manner.

In a publication by G.J. Coviello entitled "Integration of Circuit/Packet Switching by a SENET Concept", Proceedings of the National Telecommunications Conference NTC 1975, pp.42-12...42-17, a switching node is disclosed in which traffic of incoming lines is separated into two classes: Circuit-switched traffic and packet-switched traffic. Two busses are provided for the two classes to allow separate switching; voice traffic is transferred over the one bus into class I output queues, and the packets are handled as class II and transferred by a packet processor. No solution is given for the arbitration between input trunks for access to the bus for circuit-switched traffic.

European patent application 0,054,077 entitled "Method of Transmitting Information Between Stations Attached to a Unidirectional Transmission Ring", published in June 1982, describes a token ring communication system in which, besides irregular packets, also synchronous information can be transmitted by issuing a priority token in quasi-synchronous intervals. However, the beginning of synchronous information transfer has to wait for the termination of any packet transmission in progress. The system is designed for locally interconnecting stations, and not as a switching node for interconnecting lines or trunks.

An article by T.Takeuchi et al. "An Experimental Synchronous Composite Packet Switching System", published in the Proceedings of the IEEE 1986 International Zurich Seminar on Digital Communications, pp.149-153, describes a system for common handling of circuit-switched and packet-switched traffic. Multiple switch modules are interconnected by a high-speed ring. CS data from several channels are collected in composite packets which are sent from one module to another with an address. However, actual switching is done in these modules by slot interchange procedures as usual in TDM switching systems. Actual transfer of information over the ring is done in equal-length baskets so that the composite CS packets as well as non-composite data packets must be partitioned into equal-length sections with additional sequence numbering. When circuit-switched calls are terminated, a rearrangement of all slots in the composite packets is necessary.

OBJECT OF THE INVENTION

It is the object of the invention to provide a switching method and exchange apparatus which can handle synchronous or circuit-switched as well as asynchronous or packet-switched traffic; which has a relatively simple structure; needs only a single common data bus and no ring transmission medium; is flexible with respect to the necessary rearrangements when connections are finished or established; and allows a modular design.

DISCLOSURE OF THE INVENTION

The novel switching method and apparatus of the invention for achieving these objects are defined in independent claims 1 and 11.

Advantages of the solution proposed by the invention are that idle circuit-switched capacity is immediately released for data packet traffic, that no time-slot rearrangement and related signalling procedures are needed, that a simple voice input/output organization is used, and that synchronous channels of various speeds can easily be supported.

Further features and advantages of the invention will become apparent from the following detailed description of a preferred embodiment in connection with the accompanying drawings.

LIST OF DRAWINGS

Fig.1 is an overview of a switching exchange in which present invention is used;

Fig.2 shows the basic frame format for information transmission on the data bus of Fig.1;

Fig.3 illustrates details of buffering in the FIFO buffers of Fig.1;

Fig.4 is a detailed illustration of the frame format on the data bus;

Fig.5 is a schematic representation of the bus system in the exchange of Fig.1, including data bus and access control lines;

Fig.6 shows the bypass/insert switch used in the access control lines of the bus system in Fig.5;

Fig.7 shows the timing and control signals at the interface between the bus controller and the access control lines;

Fig.8 is a block diagram of the circuitry for the assembly of minipackets;

Fig.9 is a time diagram illustrating the assembling of minipackets, including local addresses and tags;

Fig.10 is a block diagram of the circuitry for readout of minipackets form FIFO buffers;

Fig.11 is a time diagram illustrating the readout of minipackets from FIFO buffers;

Fig.12 is a block diagram of the circuitry for editing PS data packets;

Fig.12 is a time diagram illustrating the editing and transfer of PS data packets;

Fig.14 is a block disgram of the circuitry for readout of PS data packets from FIFO buffers;

Fig.15 is a schematic representation of a multiple bus extended exchange configuration.

DETAILED DESCRIPTION

1) SYSTEM OVERVIEW

Fig.1 is the basic outline of a switching exchange in which the invention is used. The exchange interconnects a multiplicity of communication lines (channels) 11A, 11B for circuit-switched (CS) or synchronous traffic, e.g. voice transmission lines, and also lines 13A, 13B for packet switched (PS) or asynchronous traffic, e.g. lines for computer data. Incoming CS lines 11A are connected to CS input port units 15A, and outgoing CS lines 11B originate in CS output port units 15B. Similarly, incoming and outgoing PS lines 13A and 13B are connected to the exchange by PS input port units 17A and PS output port units 17B, respectively. There are also mixed input port units 19A which can be connected to both, CS input lines 11A and PS input lines 13A, and mixed output port units 19B which can be connected to both, CS ouput lines 11B and PS output lines 13B. For packaging purposes, a pair of input and output port units, e.g.15A and 15B, would be placed on one port circuit card (15).

Each of the port units for single traffic type (15A, 15B, 17A, 17B) includes one first-in/first-out (FIFO) buffer in which the incoming or outgoing information is temporarily stored. Each of the mixed port units (19A, 19B) includes a pair of FIFO buffers: One for the CS traffic, and one for the PS traffic.

All port units are interconnected by a data and address bus 23 (which will be termed "data bus" for short in the following description). A bus controller 25 is provided which controls the readout of information (CS samples or PS data packets) from the input port units for their transfer to the destination output port units. For this purpose, bus controller 25 is connected to all port units by access control lines 27, but it is also connected to the data bus 23.

It should be noted that the term "data" is used in the following often in its broader sense, i.e. including, besides actual data, also addresses and error checking information, if a distinction is not necessary in a particular situation (e.g. if a gating circuit is opened for all of these "data").

Operation principle is as follows: CS data or voice samples (termed "CS data" for short in the sequel) which are incoming on the CS lines are assembled into minipackets in the respective input port unit, and a local routing address is attached to each minipacket. This address designates the output port unit and the respective outgoing CS line for the information (data bytes or voice samples) of the respective minipacket. Minipackets are stored sequentially in the CS FIFO buffer of the respective input port unit. Each minipacket holds only samples of one CS channel (i.e. samples having the same destination).

If an incoming CS line 11A carries time division multiplexed traffic of several CS channels, they could use the same minipacket if all the channels were to be further transferred on the same output of the exchange (group switching). Otherwise, for each channel a separate minipacket with an individual local routing address would have to be generated. To simplify the description, it is assumed that each CS input line 11A carries only one channel (is not time-divison multiplexed).

Each packet which arrives on an incoming PS line is first assembled in a packet assembler and then stored in the PS FIFO buffer of the respective input port unit, after attaching a local routing address to it.

Transfer of data from input ports to output ports is effected as follows in accordance with the invention: The bus controller defines time frames on the bus which are of constant length. Each time frame is separated into a CS portion having CS time slots, and a PS window in which data packets of varying length are transmitted, as shown in Fig.2. The boundary between CS portion and PS window is variable, the length of the CS portion, i.e. the number of CS slots, corresponds to the number of presently active CS channels.

Under control of the bus controller 25, all CS FIFO buffers of input port units are selected sequentially once during each frame period, and all minipackets of each FIFO buffer which arrived during the last frame period are read out to the data bus. The output port units accept the minipackets according to their local routing address (first part), and place them in the CS FIFO buffer from where they are read out and gated to the proper CS output line as determined by the second part of the minipacket's local routing address. At the end of the CS portion of each frame, an access mechanism is started for the PS input port units (and mixed input port units) by which access to the data bus is granted to one of them for transmitting a data packet in the PS window of the frame. If at the end of one packet transmission, time is left in the PS window, the access procedure is resumed and another packet transmission can be started.

It is one feature of the proposed system that at the end of each frame, i.e. in exactly periodic intervals, a new frame is started regardless whether a packet transmission is in progress or not. If a packet is just being transmitted at the end of a frame, the PS transmission is interrupted with the next byte to allow immediate starting of CS FIFO buffer readout for CS minipacket transfer. At the end of the CS portion, i.e. after serving all CS FIFO buffers once, the next PS window starts and the transmission of the interrupted packet is resumed. At the end of the transfer of the interrupted packet, the access mechanism is started again (if there is still some time left in the respective PS window).

2) DETAILS OF AN IMPLEMENTATION

More details of a switching exchange implementing the present invention are now described with reference to Figs.3 and 4. In these figures, details of the access mechanism are not shown; they will be described separately in connection with Figs.5 through 7, 10, 11, and 14.

Fig.3 illustrates how CS minipackets and PS data packets are stored in the FIFO buffers, and how they are extracted from the data bus. This figure shows only one CS input port unit, one CS output port unit, one PS input port unit, and one PS output port unit.

Each CS input port unit 15A (Fig.1) comprises a multiplexer and assembly unit 31 to which a plurality of CS input lines 11A (e.g. 16 lines) are connected, and one FIFO buffer 33. The assembly unit 31 collects the CS data (voice samples) arriving on each line 11A separately, and at the end of each frame period, it attaches the correct local routing address to the sequence of CS bytes (voice samples) and transfers each such sequence as a minipacket into the associated FIFO buffer 33. The minipackets are stored in parallel byte format; i.e. each row of the FIFO buffer stores in parallel the eight bits of one byte, plus a two-bit tag which is attached to each byte in the assembly unit. These tags serve for identifying start and end of each minipacket (as will be explained later), and in particular, one of the tags is an end tag which designates the end of the last minipacket of each minipacket group belonging to one frame period. Assembly unit 31 for assembling the minipackets and for attaching a tag to each byte will be described in a later section.

In the present example, each local routing address consists of two bytes, one for the output port unit, and the other one for the output line. (Some of the two-byte local routing addresses could also be broadcast or group selection addresses.) The CS data (or voice sample) section of each minipacket holds several bytes (e.g. eight voice samples). Any number of bytes can of course be selected for the address and for

the data section, depending on the application for which the respective exchange is used.

In addition to the two local routing address bytes, a third address byte could be provided to distinguish e.g. between several exchange modules which might be interconnected to increase capacity, as will be briefly explained in a later section. Furthermore, a control byte could be appended to each minipacket (together with the local routing address bytes) to enable the selection of specific functions within the exchange, such as priority handling or the like.

As is shown in Fig.3, each FIFO buffer 33 holds in sequential order for each minipacket group, the address (A) of the first minipacket (2 bytes), then the data section (V) of the first minipacket (several bytes), immediately thereafter the address of the second minipacket, followed by the data section of the second minipacket, and so on. The last data byte of the last minipacket of one group holds the end tag. One advantage of this design is that minipackets of the next group, i.e. those belonging to the following frame, can be stored immediately after the minipackets of the previous group, because readout is effected only up to the end tag in one readout operation. If the connection in one channel is terminated in a frame period, or if a new connection is established, no adaptation is required with respect to the FIFO buffers and their readout mechanism.

It should be noted here that for the present example, it was assumed that all minipackets have the same length, i.e. slots in the CS portion of each frame are all equal. If different transmission speeds are used on the different CS transmission lines 11A, the following is possible:

(a) the assembly unit 31 generates uniform CS minipackets. This will result e.g. in the following situation: For a fast line, four minipackets will be generated in each frame period; for a medium line, only one minipacket will be formed per frame; and for a slow line, a minipacket will only be completed in every second frame period. The FIFO buffer readout mechanism described will easily handle this situation.

(b) The assembly unit 31 generates one and only one minipacket per input line in each frame period, but the minipacket length corresponds to the respective line speed. Also this situation is easily handled by the described readout and minipacket transfer mechanism.

Each CS output port unit 15B includes, besides a FIFO buffer 35 which is identical to the FIFO buffer in the input port unit, an address decoder 37 and a gating circuit 39. The address decoder can recognize, besides the own unit's local address, a minipacket start tag (identifying a first local address byte), and a minipacket end tag. The address decoder also receives a CS/PS control signal by which it is only enabled during the CS portion of each frame. The CS output port unit further includes a demultiplexer/disassembler unit 41 which extracts minipackets from the associated FIFO buffer 35 and distributes the samples to the CS output lines 11B, depending on the local routing address found with the minipacket, and in correct timing as required for each of the CS output channels. Local routing address bytes and all two-bit tags are eliminated in the demultiplexer/disassembler.

When a minipacket group is read out from a CS FIFO buffer 33, the bytes appear sequentially on data bus 23. Each address decoder 37 looks for a first local address byte to appear on the bus (recognizable by the unique start tag), and if the respective address byte corresponds to the address of the respective output port unit, the whole minipacket (up to a minipacket end tag) is gated into the associated CS FIFO buffer 35. Thus, the minipackets of one group are correctly distributed to their intended destination output units.

PS input port units 17A are similar to the CS input port units, except for the assembling of minipackets. Each PS input port unit comprises a multiplexer and packet assembler 43 to which several PS transmission lines 13A are connected, and which has one output connected to a packet editor 45 which in turn is connected to the input of the PS FIFO buffer 47. Whenever a complete packet is available for switching, the packet assembler 43 sends a ready signal and then the assembled packet to the packet editor 45 by which a local routing address (two bytes in present example) is derived from the packet system destination address and is appended to the received packet during its transfer to the FIFO buffer. The data packet as received, including the system destination address, source address, error checking characters, etc. is not changed. Each byte of the packet plus the two local routing address bytes, is extended by a two-bit tag, as was explained already for the CS minipackets. This is also achieved by the packet editor 45 during transfer of the packet to the FIFO buffer. The different tags and their meanings are explained in a later section. Details of the packet editor will also be disclosed in a later section.

PS output port units 17B are very similar to the CS output port units. They also contain an address decoder 49 (which can recognize the local routing address of that unit, as well as a packet start tag and two different end tags), a gating circuit 51, FIFO buffer 53, and a demultiplexer/packet disassembler 55 connected to several PS output lines 13B. Address decoder 49 also receives a CS/PS control signal by which it is enabled only during the PS window of each frame. The demultiplexer/packet disassembler reads out available packets from the FIFO buffer 53 and gates each packet to the correct output line 13B, as indicated by the second local routing address byte accompanying the packet. The local address bytes and

the two-bit tags are of course striped off before the packet is released on a transmission line.

When a PS input port unit is selected for a packet transfer, the respective FIFO buffer 47 is read out to the bus until the byte with the packet end tag appears. The address decoders 49 in PS output port units detect any first local address byte appearing on the data bus, and if the local routing address corresponds to the unit's address, the whole packet up to the packet end tag is then gated to the associated PS FIFO buffer.

The handling of interrupted packet transfers will be explained in a later section. However, it can be mentioned here that address decoder 47, when receiving an intermediate end tag (issued when a packet is interrupted), disables gating circuit 51 but is kept in a wait state. When the address decoder, being in wait state, receives another start tag during a PS window, it enables gating circuit 51 again until it receives the final end tag of the respective packet.

Fig.4 illustrates the contents of two consecutive frames i and i+1 on the data bus. As can be seen, the first portion of each frame always contains a train of CS slots, each slot carrying one minipacket. The number of slots adapts to the number of presently active CS channels. A short gap (equal e.g. to one slot time) may appear after each group of CS slots from one FIFO buffer, to allow for switching from one input port unit to the next (daisy-chain forwarding) during the packet readout procedure. Packets are transferred in the PS window as they become available. As can be seen, a whole packet transfer may fit into one PS window, or it may be necessary to interrupt one packet transfer at the end of a frame and resume the suspended transfer after the CS slots of the next frame. There may also be idling portions in the PS windows if no packets are ready for transfer.

3) BUS SYSTEM AND ACCESS CONTROLS

Fig.5 depicts the bus system and access control lines for the present embodiment of the invention. In the figure there can be seen the bus controller 25, one port circuit card 57 (which is exemplary for a plurality of similar cards), the data bus 23, access control lines 27, and an optional bus repeater 59. Each of the port circuit cards may either contain one pair of port units (e.g. 15A and 15B) or a group of such port unit pairs. The data bus lines and access control lines connected to the respective port circuit card are internally connected to each of the individual port units, as required.

The data bus is split into two portions, a transmit bus 23A and a receive bus 23B. Each bus consists of 10 parallel bit lines, for carrying the eight bits of each minipacket/data packet byte transmitted, plus the two appended tag bits. Instead of a separate transmit and receive data bus, of course a single bidirectional data bus 23 could be used as is generally shown in Fig.1, but the split bus allows faster operation.

The access control lines are actually one bus line and two loop lines originating in the bus controller 25, going through each connected port unit, and returning back to the bus controller. The three different access control lines are:

(a) A CS/PS window indicator bus line 61. The binary signal on this line indicates the present status of the frame on the data bus, i.e. whether currently a CS slot transmission is active, or whether the PS window is open.

(b) A CS access control line 63. This is a loop line or daisy-chain line for selecting sequentially, during the CS slot portion of each frame, all CS FIFO buffers in CS input port units 15A and in mixed input port units 19A. This line is connected to each port unit card by an insert/bypass switch 67 which is shown in detail in Fig.6. Without an attached port unit card, the respective switch 67 bypasses that location, i.e. the loop line is then not interrupted at the switch. When any port unit card is activated, the bypass switch is opened and the input port units on the respective card which have CS FIFO buffers are inserted into the loop. Operation of the CS access control (daisy-chain) is explained later.

(c) A PS access control line 65. This line is a token loop line for transferring a token which grants access to the data bus for packet transfer during the PS window of a frame. This loop line is also connected to the port unit cards by insert/bypass switches 67, so that a location can either be bypassed, or the token ring line is opened and all input port units of the respective card having PS FIFO buffers are inserted into the loop line. Operation of the token arbitration mechanism will also be explained later.

A time diagram of the signals on these three access control lines, as they leave or enter, respectively, the bus controller 25, is shown in Fig.7. At the beginning of a frame period, the bus controller issues a short pulse on the daisy-chain line 63. This will cause readout of the first CS FIFO buffer. The pulse is passed on through all CS input port units (as will be shown in connection with Fig.10), and finally returns from the last CS input port unit on the loop to the bus controller. This ends the CS slot portion of the frame. The PS window is then started by the bus controller, by releasing a token which is a particular bit sequence on the

token loop line and by changing the CS/PS window indicator signal on line 61 to its low level. The token passes through the PS input port units and is seized by any such unit which has a data packet ready for transmission. The token is released by the respective PS input port unit after the packet transmission, for further propagation on the token loop line, and may finally return to the bus controller in the same frame period. However, if a packet transmission is not finished before the start time of the next frame period, that transmission will be suspended, the token will be kept by the respective PS input port unit and thus will not return to the bus controller in that frame.

The CS transmission portion of the new frame starts by releasing another daisy-chain pulse from the bus controller and by raising the CS/PS window indicator signal. Another cycle of CS FIFO buffer readout operations is executed.

At the beginning of the next PS window (i.e. when the daisy-chain pulse returns to the bus controller), the bus controller will lower the CS/PS window indicator signal on access control line 61, but it will release a token only if in the last frame period, a token returned to it. Otherwise, the interrupted packet transmission will be resumed by the interrupted PS input port unit, which will later, after the packet transmission ends, release the token on loop line 65. To resume: The CS/PS window indicator signal, and the outgoing daisy-chain pulse are periodic signals, whereas timing of the other three signals depends on the number of active CS channels (daisy-chain incoming pulse and outgoing token) and on the packet traffic (outgoing token and incoming token).

Alternative solutions are of course possible for the arbitration schemes. The daisy-chain signal could be a DC level signal instead of a pulse signal. The token for PS arbitration could be a single-bit token instead of a multiple-bit token. If a multiple-bit token is used as shown for above example, one could also include address information or priority information in the token. Furthermore, the same arbitration scheme could be used for the CS and PS switching procedures (either a daisy-chain scheme for both, or a token mechanism for both, or any other suitable access control scheme).

Clock signals are of course transferred from the bus controller to all port units, for synchronizing the bit transfers on the data bus. No details are shown because such clocking is well known in the art. It should be noted that when the data bus lines 23 and the clock lines are installed as parallel lines, the data delay and clock signal delay would be alwys the same for any one port unit attached to the data bus and the clock lines.

4) ASSEMBLY UNIT IN CS INPUT PORT UNIT

Fig.8 is a block diagram of the assembly unit 31 which is provided in each CS input port unit 15A and in each mixed input port unit 19A for assembling minipackets including local routing addresses, and for appending a two-bit tag to each byte. For each of the input lines (channels) 11A(1) to 11A(n), a pair of assembly buffers 71A/71B is provided which are selected alternatingly for writing and reading by selector switches 73A and 73B. During one frame cycle, one of the buffers collects the CS data bits or voice samples arriving on the line, while the other buffer is read out. (For analog input lines, digital voice samples are produced by well-known A/D conversion.) Further provided are sixteen local routing address registers 75(1) to 75(n). For each connection that exists, a local routing address is held in the address register associated with the repective input line (channel). Furthermore, there are four two-bit tag registers 77A, 77B, 77C and 77D for holding the tags 00, 01, 10 and 11.

Selector circuits 79, 81 and 83 are provided for selecting either one of the address registers 75 or one of the buffer pairs 71A/B as a source for data on the eight parallel bit lines 85. Another selector circuit 87 is provided for selecting one of the four tag registers 77A/B/C/D as source for data on the two parallel bit lines 89. The data of lines 85 and 89 are combined in gating multiplexer 91 to form a ten-bit input to the FIFO buffer 33 of the respective CS input port unit 15A. Gate timing means 69 furnishes control signals to the selector and multiplexing/gating circuits so that in a readout cycle for the respective CS input port unit, for each active input line first two address bytes and then all CS data bytes (voice samples) collected during one frame period are transferred to the FIFO buffer, with two appropriate tag bits attached to each byte.

Table 1 given below illustrates the sequence of control signals which are issued by gate timing means 69.

Table 1 Gating Signals in the Circuitry of Fig.8

<------------ Frame i ------------> <----- Frame (i+1) ------> <----

IG	0-------	---------	---	--------0	1--------	---	--------1	0----
OG	1-------	---------	---	--------1	0--------	---	--------0	1----
LS	0-------0	1-------1	2--	7-------7	0-------0	1--	7-------7	1----
AD	001----1	001----1	001	001----1	001----1	001	001----1	001--
TS	10----02	10----02	10-	10----03	10----02	10-	10----03	10---
GM	1-------	---------	---	--------1	1--------	---	--------1	1----
GM'	1-------	---------	---	--------1	0-------0	1--	--------1	0----

IG = In Gate OG = Out Gate (0=upper / 1=lower)
LS = Line Select (for lines 0...7)
AD = Select Address or Data (0=Adress / 1=Data)
TS = Tag Select (0=Norm / 1=Start / 2=MP End / 3=CS End)
GM = Gate Multiplexer

The lines GM and GM' in this table show how simple it is with the present invention to adapt to changing traffic conditions without having to adapt many tables or circuits. With signal GM, it is assumed that all input lines are active; therefore, the gating multiplexer 91 is opened for all line intervals, i.e. during the whole frame period. With signal GM', it is assumed that the connection on line 0 is cancelled at the end of frame i; therefore, gating multiplexer 91 is closed during the time interval for line 0, beginning with frame (i+1). Nothing is transferred into the FIFO buffer during this time, but no gap will occur when the FIFO buffer is finally read out. Thus, no slot rearrangement is necessary. Similarly, interval times for the various lines can be easily adapted by changing the respective gating signals only for the line time period involved. But the CS end tag (3 in the table) must be given in the time interval of the last active input line.

Fig.9 is a time diagram illustrating the assembling of minipackets in the FIFO buffer. Each block designated A(i) is one local routing address byte, and each block designated D(i) is one CS data byte/voice

sample. The two-bit tags attached to each byte have the following meaning:

00 = Normal address byte or data byte
01 = Start of minipacket (first address byte)
10 = End of normal minipacket (last data byte)
11 = End of last minipacket in a train of minipackets belonging to one frame period = CS end tag

To simplify the description, only the assembling of minipackets of uniform length and for equal-speed input lines was described here. As was indicated already earlier, the described assembly scheme could also handle traffic of input lines with different speeds. If equal-size minipackets are used, the timing signals would have to cause emptying of the higher-speed line input buffers 71A/B in each frame period, whereas the lower-speed line input buffers 71A/B would be emptyed only e.g. every second or fourth frame period. Alternatively, if all input buffers were to be read out in each frame cycle, the minipackets assembling in the input buffers 71A/B would be automatically shorter for slower input lines and longer for input lines with higher speed.

5) FIFO BUFFER READOUT CONTROL IN A CS INPUT PORT UNIT

Fig.10 shows the circuitry by which the readout of a CS input FIFO buffer is controlled once in each frame period in response to the daisy-chain signal on the CS access control line 63. It comprises readout control means 93, a CS end tag decoder 95, and a switch 97 for applying a select pulse to the outgoing daisy-chain line 63. Inputs of the readout control means 93 are connected to the incoming daisy chain line 63 and to the output of the CS end tag decoder 95. Output control lines of the readout control means are connected to the switch 97 and to the readout control input of the FIFO buffer 33. Input of the CS end tag decoder is connected to the output line of the FIFO buffer 33.

Operation of this circuitry is explained with reference to the timing diagram of Fig.11. When a select pulse is received from the preceding CS input port unit on daisy-chain line 63, readout control means 93 raises the readout control signal on its output line so that address and data bytes are sequentially read out from the FIFO buffer 33 to the data bus 23. As soon as a CS end tag (11) is detected, i.e. when all minipackets belonging to one frame period were transferred to the data bus, a stop signal is sent to the readout control means which thereupon stops the readout signal and causes the switch 97 to send a short select pulse on the daisy chain line 63 to the next CS input port unit.

6) PS DATA PACKET EDITING

Fig.12 is a block diagram of the circuitry for editing data packets which were received on PS input lines 13A. The multiplexer and packet assembler 43 and FIFO buffer 47 were already shown in Fig.3. Data packets arriving are stored sequentially in the packet assembler without any change, including destination and source addresses and check bytes (e.g. CRC).

Packet editing circuitry 45 comprises transfer control means 101 which receives the "Packet Ready" signal on a line 99 from packet assembler 43, and issues control signals to the other units. A shift register and decoder unit 103 is provided in the data path between packet assembler 43 and FIFO buffer 47. It recognizes and transfers a packet's system destination address (SDA) to address conversion circuitry 105, and it recognizes a packet's end. Address conversion circuitry 105 has a stored address conversion table and can issue in response to a packet's system destination address the correct local routing address bytes.

Three two-bit registers 107A/B/C are provided for storing the tags 00 (normal byte), 01 (packet start/restart), and 11 (packet end). Furthermore, two selector circuits 109 and 111 and a multiplexing/gating circuit 113 are provided. They are controlled by signals from the transfer control means 101.

Operation of the packet editing circuitry is explained with reference to the timing diagram of Fig.13. The tags used for packet transfer have the following meaning:

00 = Normal packet byte or second local address byte
01 = Start of a packet transfer (first local routing address byte) or restart of a packet transfer
10 = Intermediate end of a packet transfer (interruption for CS transfer in a new frame)
11 = Final end of a packet transfer

The intermediate end tag (10) is only used in the PS FIFO readout circuitry. as will be explained in another section (in connection with Fig.14).

When a packet is transferred from packet assembler 43 to FIFO buffer 47, two local routing address bytes are first gated into the FIFO buffer through selector 109 and multiplexer 113. Simultaneously, a start tag (01) and a normal tag (00) are appended to the first and second local address byte, respectively. Thereafter, all packet bytes are transferred through selector 109 and multiplexer 113, appending a normal tag (00) to each byte. When the end of a packet was recognized, an end tag (11) is appended to the last byte of the packet. Delay of the shift register/decoder 103 and control signals of transfer control means 101 are so selected that the beginning of the data packet, i.e. its system destination address, will immediately follow tha second local routing address byte, and that the end tag is correctly appended to the last packet byte.

When a complete packet is available in the FIFO buffer, a request-to-send signal (RTS) is active on line 115.

7) FIFO BUFFER READOUT CONTROL IN A PS INPUT PORT UNIT

Fig.14 shows the circuitry by which readout of the PS FIFO buffer in a PS input port unit (or in a mixed input port unit) is controlled during the PS window portion of a frame. It comprises readout control circuitry 117, tag editing circuitry 121, a token detector 123, a token generator 125, a latch 127, and an end tag decoder 129. The incoming token loop line 65 can be connected by a switch 131 either directly to the outgoing token loop line 67, or to the token decoder 123. The switch responds to a request-to-send (RTS) signal on line 115 which is activated when a data packet was received in the PS FIFO buffer of the respective unit. When no RTS signal is active, any token is directly passed on to the next PS input port unit.

However, if RTS is active and a token is received in token detector 123, latch 127 is set and furnishes a select signal on line 133. This select signal is passed on through an AND gate 135 as a ready signal on line 137 to readout control means 117 only when the CS/PS window indicator signal on line 61 indicates that a PS window is open. Readout control circuitry 117 then activates a readout control signal on line 139 which starts a readout operation for the FIFO buffer 47. If no interruption occurs, a whole packet (lead by a two-byte local routing address) is transferred to data bus 23. When an end tag (11) is detected by end tag decoder 129, latch 127 will be reset by a signal on line 141, and the select, ready, and readout signals on lines 133, 137, 139 will be deactivated thus ending the readout process. Simultaneously, token generator 125 is activated and will transmit a token on outgoing loop line 65 to the next PS input port unit.

If, during packet transmission, the PS window is closed to allow start of a new frame, an interrupt procedure occurs: Due to a change in the CS/PS window indicator signal on line 61, the ready signal on line 137 is deactivated. The readout control circuitry will then deactivate the readout signal on line 139 when the next byte was read out, and cause tag editing circuitry 121 by a control signal on line 143 to append an intermediate end tag (10) to the last byte transferred, cf. Fig.13. The token, however, is kept by the respective PS input port unit (latch remains set).

When, after the CS transmission period, the PS window is opened again (change of signal on line 61) the ready signal on line 137 will be activated again; readout control circuitry 137 will reactivate the readout signal on line 139, and because it had not yet received an end tag indication on line 141, it will cause tag editor 121 to append to the first byte of the second portion of the packet another start tag (01) instead of the normal tag (00), cf. Fig.13.

The intermediate end tag (01) will cause the receiving PS output port unit to go into a wait state, thus interrupting reception of bytes from the data bus, and to resume reception when the PS window is opened again (signal on line 61), and when it receives from the bus a data byte having the start tag. Only when the receiving PS output port unit detects a final end tag (11) it will stop the receiving procedure.

The end of a packet transmission in the sending PS input port unit is the same for interrupted packets as for uninterrupted packets (described above).

8) MULTIPLE BUS EXPANSION OF THE SWITCH

Several exchange units such as the one described so far can be interconnected by multiple busses, as shown in Fig.15. Interbusses IB 1, IB 2, IB 3 etc. are provided, one for each exchange unit, for carrying traffic from the respective exchange unit to the other exchange units.

Each of the exchange units has to be equipped with a special IB output port unit 151(i) for transferring the traffic from the local bus 23(i) to the interbus IB(i), and with a special IB input port unit 153(i) for transferring the traffic from all other interbusses to the local bus 23(i). If there are n exchange units in total, there will be n interbusses, and each IB input port unit 153(i) is connected to (n-1) interbusses by (n-1) IB selector gates 155(ij).

Furthermore, local routing addresses used in the exchange units must be extended to have three local routing address bytes, i.e. one extra local address byte for designating the exchange unit to which the respective minipacket is to be transferred.

More details will now be explained with reference to the example shown which has altogether three exchange units. In particular, the interbus traffic from and to exchange unit 1 will be described.

IB output port unit 151(1) has an address decoder, gating circuit, and FIFO buffer equal to those shown in Fig.3 for CS output port unit 15B, but no demultiplexer/disassembler. When CS minipackets are transferred over the local bus 23(1); the adress decoder and gating circuit will transfer all minipackets destined for another exchange unit to the FIFO buffer of IB output port unit 151(1). Contents of this FIFO buffer is continously read out directly to interbus IB 1 as a serial stream of bytes. Local routing addresses and the two-bit tags are not striped off in the IB output port, they are transferred over the interbus to the other exchange units. Thus, the interbusses have 10 parallel bit lines as the local busses.

IB input port unit 153(1) has two FIFO buffers and for each of them associated access control and readout circuitry, as shown for the normal CS input port units 13A in Fig.10. (In the general case, there would be (n-1) FIFO buffers, each with associated circuitry). Each of the two IB selector gates 155(12) and 155(13) sees all the minipackets which appear on the interbus to which it is connected, but will gate only those minipackets into its connected FIFO buffer in the IB input port unit 153(1) which have a local routing address byte designating the own exchange unit 1. Thus, minipackets are collected in the FIFO buffers as it is done in the normal CS input port units. The IB selector gates contain an address decoder and a gating circuit as shown for the CS output port units in Fig.3.

The readout control means for the FIFO buffers in IB input port unit 153(1) are both connected into the daisy chain line 63 which is anyway connected to all normal input port units having CS input FIFO buffers. Thus, in the CS portion of each frame period, first all normal CS input FIFO buffers are read out (each up to the next CS end tag), and then the two FIFO buffers of the IB input port are read out in the same way, so that their contents is transferred to the different output port units connected to local bus 23(1), according to their local routing addresses.

9) OTHER ALTERNATIVE SOLUTIONS

One implementation of the invention was disclosed in the above description, but several alternatives are possible for the implementation of individual features. Three interesting alternatives will be briefly explained here.

A) Optical Bus Arrangement

Instead of electrical ten-wire busses which were assumed for the given example, one could also provide optical fiber busses. In this case, the data transfer on the busses would be all bit-serial, i.e. not ten bits in parallel as shown for the elctrical busses. This would require that either the FIFO buffers are also bit-serial (one bit wide), or that serializers and deserializers are provided at the outputs and inputs of the FIFO buffers. Furthermore, electrical/optical converters have to be provided at each interface between a bus and an input port unit or output port unit. The advantage of the optical bus solution is the extremely high transmission speed which can be achieved.

B) Serial Interbusses

If the distances between the exchange units in a multiple bus system (Fig.15) are large, it would be desirable to have single-wire interbusses for bit-serial transmission instead of the ten-wire interbusses for byte-parallel transmission. In this case, a serializer must be provided at each IB output port unit 151, and a deserializer must be provided at the input of each IB selector gate 155.

C) Separate Start and End Bytes

In the above example, a start tag is attached to the first local address byte of each minipacket (or PS packet), and an end tag is attached to the last byte of each minipacket (or PS packet), cf. Fig.9 and Fig.13. As an alternative, one could provide an extra byte for attaching the start tag, and an extra byte for attaching the end tag. The eight bits of such extra bytes could be a special pattern, e.g. a repetition of the attached tag: for a start tag 01, the associated byte would be 01010101, and for an end tag 11 the associated byte would be all ones. This solution requires some of the buffer and bus transmission capacity, but it would enhance reliability because of the increased checking possibilities, and because more time would be available for switching operations at the beginning and end of minipackets (or PS packets).

Claims

1. Method of transferring information between CS communication channels carrying synchronous information traffic and PS communication channels carrying asynchronous data packet traffic, in a switching exchange comprising CS input buffers and CS output buffers with associated control circuitry for first-in first-out sequential storage of traffic from said CS channels, and PS input buffers and PS output buffers with associated control circuitry for storage of traffic from said PS channels, all said buffers being interconnected by a bus arrangement for transferring information packets in periodic time frames,

the method comprising following steps:

(a) collecting information arriving in each CS input channel in a separate minipacket per given time unit, attaching to each minipacket a local address designating at least the CS output buffer to which the information is to be transferred;

(b) storing in each CS input buffer sequentially the minipackets for all CS input channels associated to it, attaching an end indicator to the last minipacket stored in the respective buffer in each time frame period; and

(c) once per time frame period:

-in a CS readout process, sequentially reading out to said bus arrangement, from each of said CS input buffers, all minipackets with their local addresses, up to the next minipacket with an end indicator; and

-starting, after carrying out the CS readont process for all CS input buffers, a window for data packet transmission between PS buffers through said bus under a predetermined arbitration-scheme.

2. Method in accordance with claim 1, further including in step (c):

-when starting said data packet transmission window, either releasing a contention procedure between said PS input buffers for transferring a data packet, or resuming a previously interrupted data packet transmission; and

-closing said data packet transmission window and temporarily interrupting any data packet transmission in progress, for starting step (c) of the next time frame period.

3. Method in accordance with claim 1, including further the step of:

storing information arriving in PS input channels, in said PS input buffers in the form of data packets as received, and attaching a local address to each data packet, designating at least the PS output buffer to which said data packet is to be transferred.

4. Method in accordance with claim 1, including the further step of:

attaching a plural-bit tag to each information byte in each minipacket when storing it into a CS input buffer, for uniquely designating the start and end of each minipacket and the last byte of the last minipacket stored in a CS input buffer within any time frame period.

5. Method in accordance with claim 1, further including the following steps:

starting a CS readout process for sequentially reading out minipackets from all CS input buffers in a predetermined sequence, at the beginning of each time frame period, by transferring a daisy-chain signal to the control circuitry of the first CS input buffer in said sequence;

furnishing a daisy-chain signal from the control circuitry of each CS input buffer, when finishing minipacket readout at occurrence of the end indicator, to the control circuitry of the next CS input buffer in said sequence, until the control circuitry of the last CS input buffer in said sequence furnishes a daisy-chain signal indicating the end of the CS readout process; and

starting a data packet transmission window in response to the daisy-chain signal from the control circuitry of said last CS input buffer.

6. Method in accordance with claim 5, further including the step of:

furnishing a binary CS/PS window indicator signal at least to the control circuitry of all PS input and output buffers, said signal assuming its one binary value at the beginning of each time frame period when the CS readout process is started, and changing to its other binary value when the end of the CS readout process is indicated and the data packet transmission window is started.

7. Method in accordance with claim 5, comprising the further steps of:

providing a token access procedure for access arbitration between the control circuitry of all PS input buffers in a predetermined sequence; and

starting a data packet transmission process at the beginning of the data packet transmission window by either releasing an access token to the control circuitry of the first PS input buffer in said sequence, or by resuming an interrupted packet transmission between a pair of PS buffers for which the packet transmission was interrupted, in response to a change in the CS/PS window indicator signal.

8. Method in accordance with claim 1, further including the following step:

interrupting, when the data packet transmission window starts, any ongoing packet transmission from a PS input buffer over the bus to a PS output buffer, and setting the control circuitry of the transmitting PS input buffer and of the receiving PS input buffer into a wait state.

9. Method in accordance with claim 8, further including the following step:

appending a particular tag to the last byte of the first portion of an interrupted data packet indicating an intermediate end, and appending a start indicating tag to the first byte of the second portion of an interrupted data packet when the transmission is resumed.

10. Method in accordance with claim 1 or claim 3, characterized in that the attached local address has at least two portions, one portion designating the output buffer to which the minipacket or data packet is to be transferred, and the other portion designating one of several output channels which are connected to the respective output buffer, and that these addresss portions are also stored in the respective output buffer.

11. Switching exchange apparatus for interconnecting communication lines (11A, 11B, 13A, 13B) carrying synchronous information traffic (CS), or asynchronous data packets (PS), said communication lines being connected to CS input and output buffers (33, 35) and PS input and output buffers (47, 55), respectively, in said exchange apparatus,

characterized by

-a bus arrangement interconnecting all said input and output buffers and comprising:

- data bus lines (23) for transferring data and addresses,
- a CS access control line (63) for the CS input buffers,
- a PS access control line (65) for the PS input buffers;

-first control means (Fig.8) for each CS input buffer, for accumulating minipackets of synchronous information (CS) received on associated input lines (11A) separately for each destination output line (11B) and for storing them in the respective CS input buffer; for attaching a local routing address to each minipacket; and for attaching an end indicator to the last minipacket stored in the CS input buffer in each time frame period;

-second control means (Fig.10) for each CS input buffer for sequentially reading out, in response to an active signal on said CS access control line (63), minipackets from said CS buffer onto said data bus lines until a minipacket with an end indicator occured; and for changing the control signal on said CS access control line so that the next CS buffer in a predetermined sequence receives an active signal on said line;

-third control means (25) in said exchange apparatus for activating a window control signal when all said CS input buffers were read out in response to a control signal on said access control line; and

-fourth control means (Fig.14) for each said PS input buffer, for transmitting in response to the reception of an access authorization on said PS access control line (65), a data packet with a local routing address onto said data bus lines, or for resuming a previously interrupted data packet transmission in response to said window control signal.

12. Switching exchange apparatus in accordance with claim 11, characterized in that a CS/PS window indicator line (61) is provided in said bus arrangement and is connected to said third control means (25) and to each of said fourth control means.

13. Switching exchange apparatus in accordance with claim 11, characterized in that a controller (25) is provided for releasing a daisy-chain signal on said CS access control line (63) at the beginning of each time frame period, and for releasing an access token on said PS access control line (65) when said window control signal is activated, if no data packet transmission interruption occured in the last frame period.

14. Switching exchange apparatus in accordance with claim 13, characterized in that said CS access control line (63) and said PS access control line (65) each form a closed loop beginning and ending in said controller (25); said CS access control line being sequentially connected to all second control means, and said PS access control line being sequentially connected to all fourth control means.

15. Switching exchange apparatus in accordance with claim 11, characterized in that all CS input buffers (33) and CS output buffers (35) are first-in first-out buffers for sequential storage of bit-parallel bytes.

16. Switching exchange apparatus in accordance with claim 11, characterized in that each said first control means comprises means for attaching a plural-bit tag to each byte which is stored into the associated CS input buffer, one of said tags being said end indicator (11), and another on of said tags being an indicator (01) for the start of a minipacket.

17. Switching exchange apparatus in accordance with claim 11, characterized in that means (117, 121) are provided in said fourth control means for entering a wait state when a data packet transmission must be interrupted at the end of a data packet transmission window; for attaching an intermediate end indicator (10) to the end of the first portion of the interrupted packet; and for attaching a start indicator (01) to the beginning of the second portion of an interrupted packet when the data packet transmission is resumed.

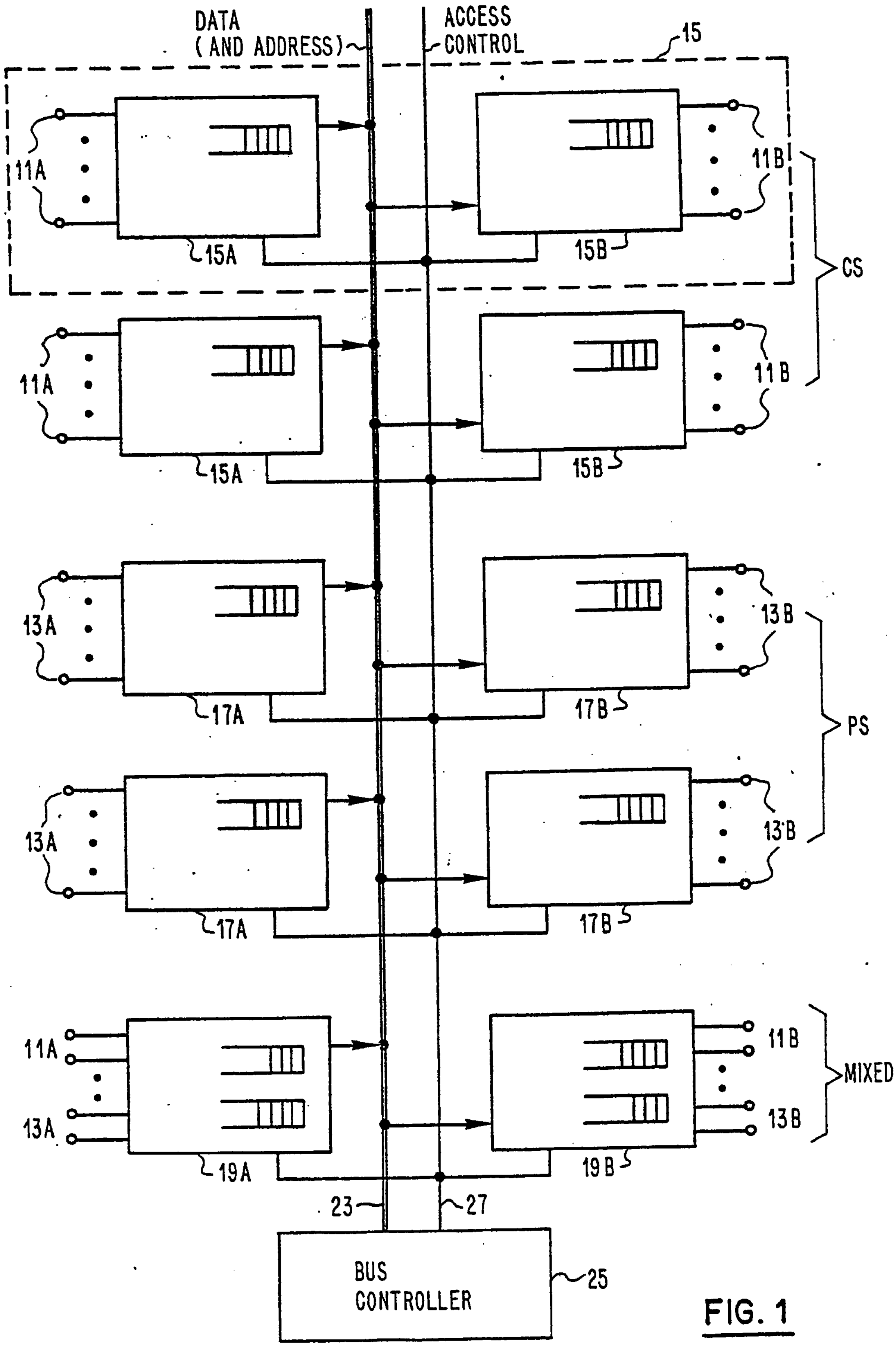

DATA
(AND ADDRESS)
ACCESS
CONTROL
15
11A
15A
11B
15B
CS
11A
15A
11B
15B
13A
17A
13B
17B
PS
13A
17A
13B
17B
11A
13A
19A
11B
13B
MIXED
19B
23
27
BUS
CONTROLLER
25

FIG. 1

FIG. 2

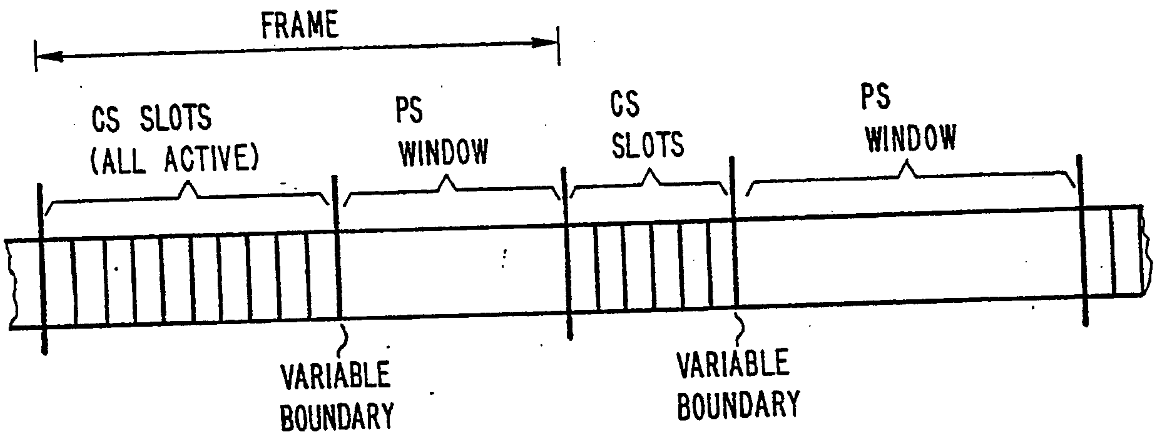
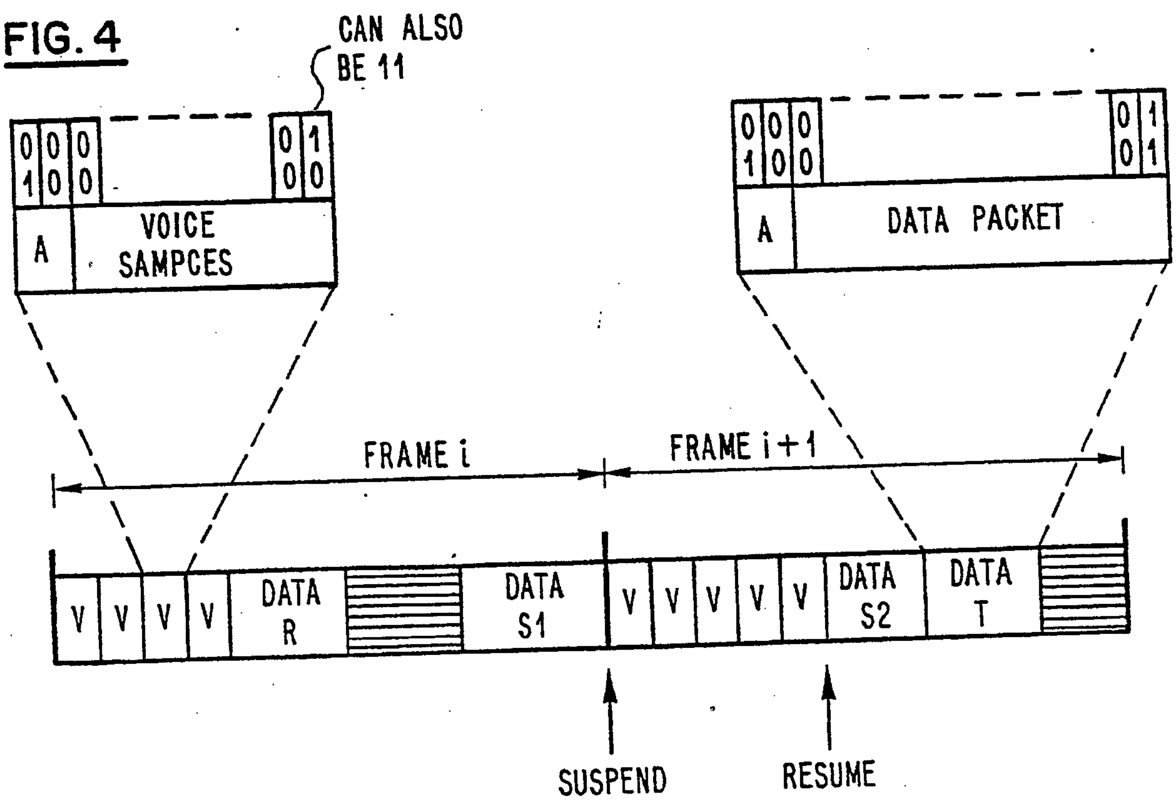
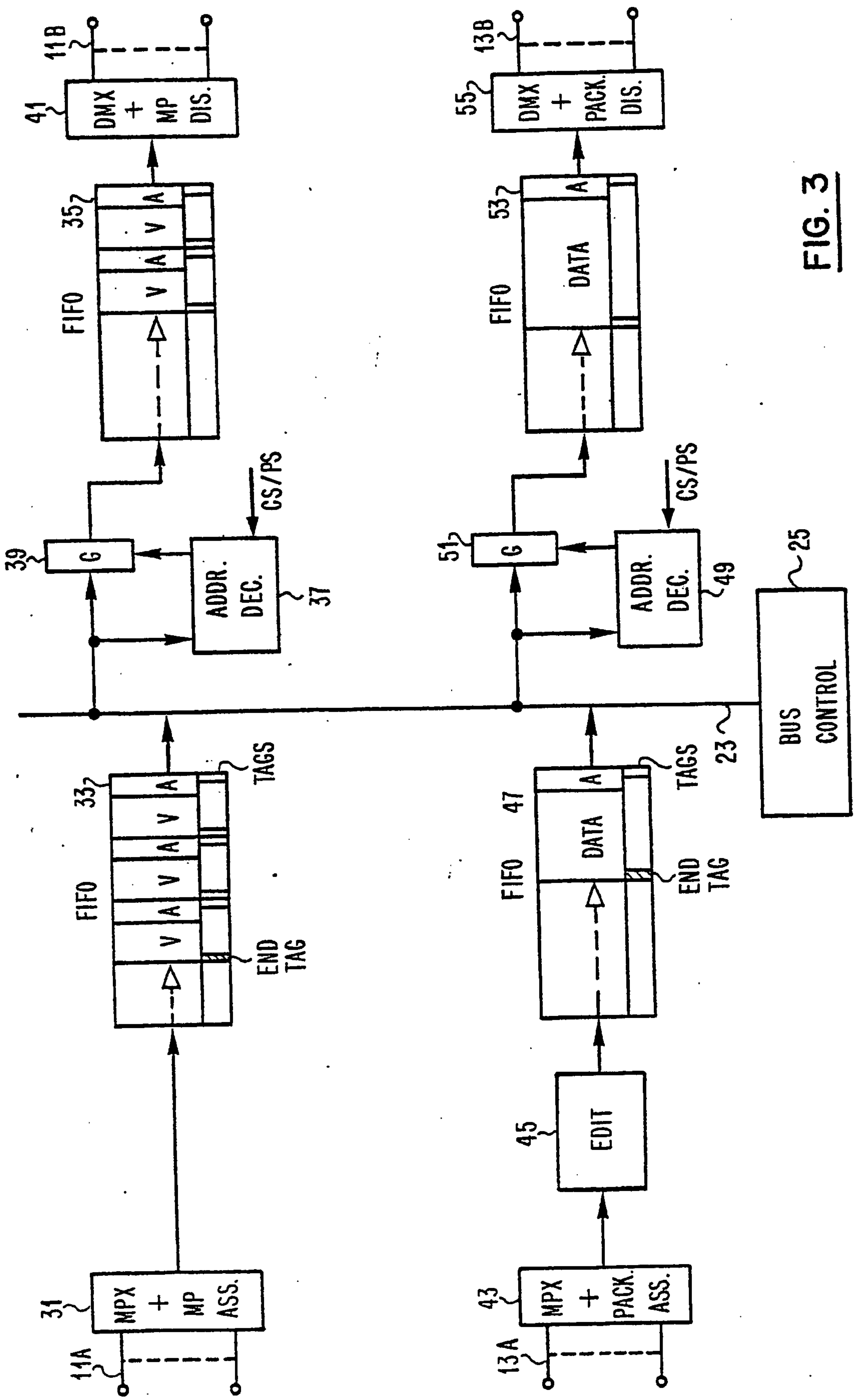


FIG. 4

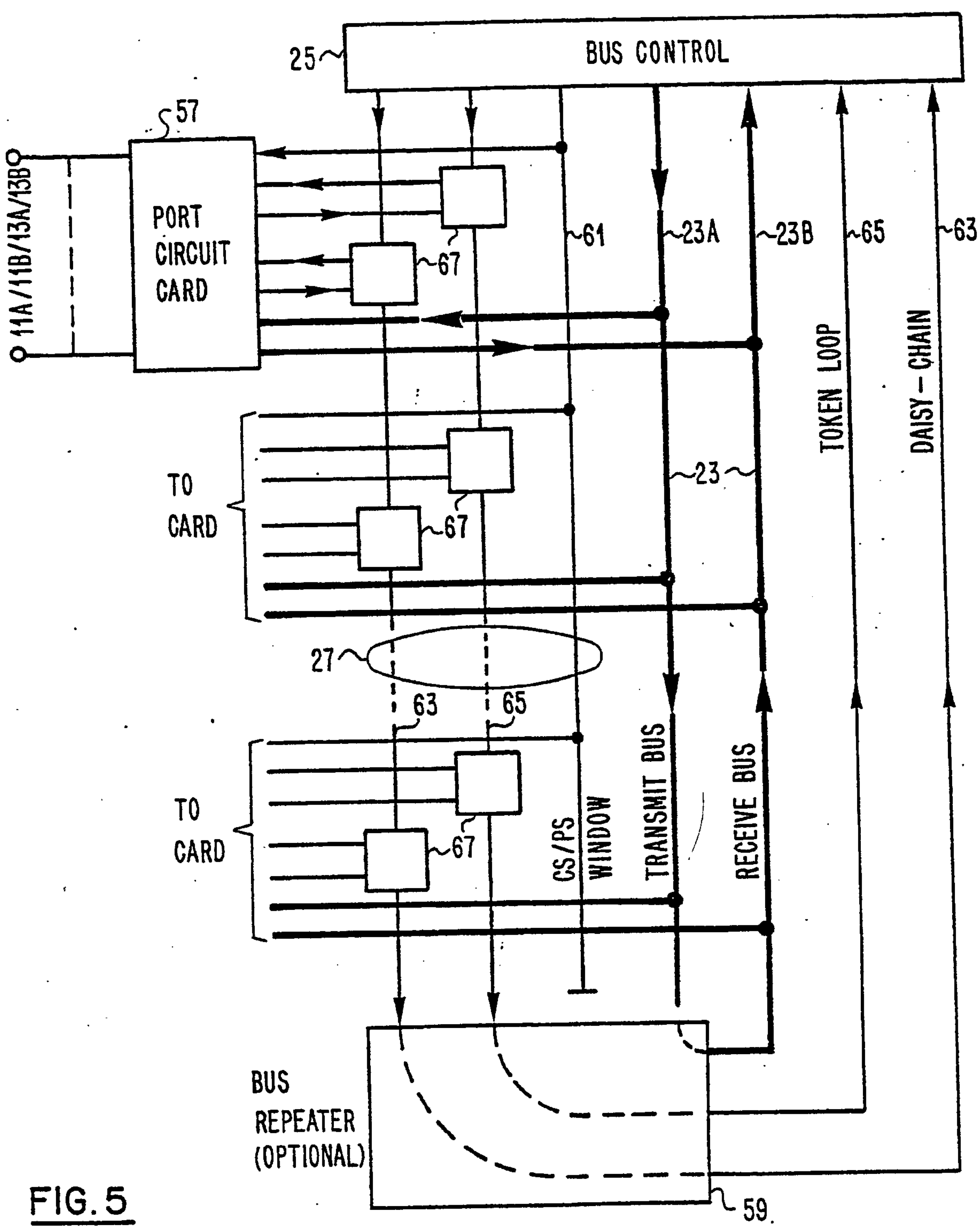


PACKET TRANSMISSION



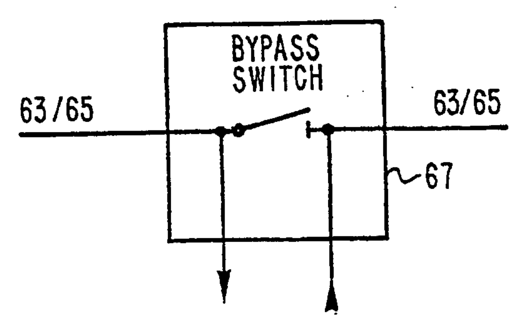
11A
31
MPX + MP ASS.
FIFO
33
V A V A V A
END TAG
TAGS
39
G
ADDR. DEC.
37
CS/PS
FIFO
35
V A V A
41
DMX + MP DIS.
11B
13A
43
MPX + PACK. ASS.
45
EDIT
FIFO
47
DATA A
END TAG
TAGS
23
51
G
ADDR. DEC.
49
CS/PS
FIFO
53
DATA A
55
DMX + PACK. DIS.
13B
BUS CONTROL
25

FIG. 3



BUS CONTROL
25
57
PORT CIRCUIT CARD
11A/11B/13A/13B
67
61
23A
23B
65
63
TOKEN LOOP
DAISY-CHAIN
TO CARD
23
27
63
65
CS/PS WINDOW
TRANSMIT BUS
RECEIVE BUS
BUS REPEATER (OPTIONAL)
59

FIG. 5



BYPASS SWITCH
63/65
63/65
67

FIG. 6

FIG. 7

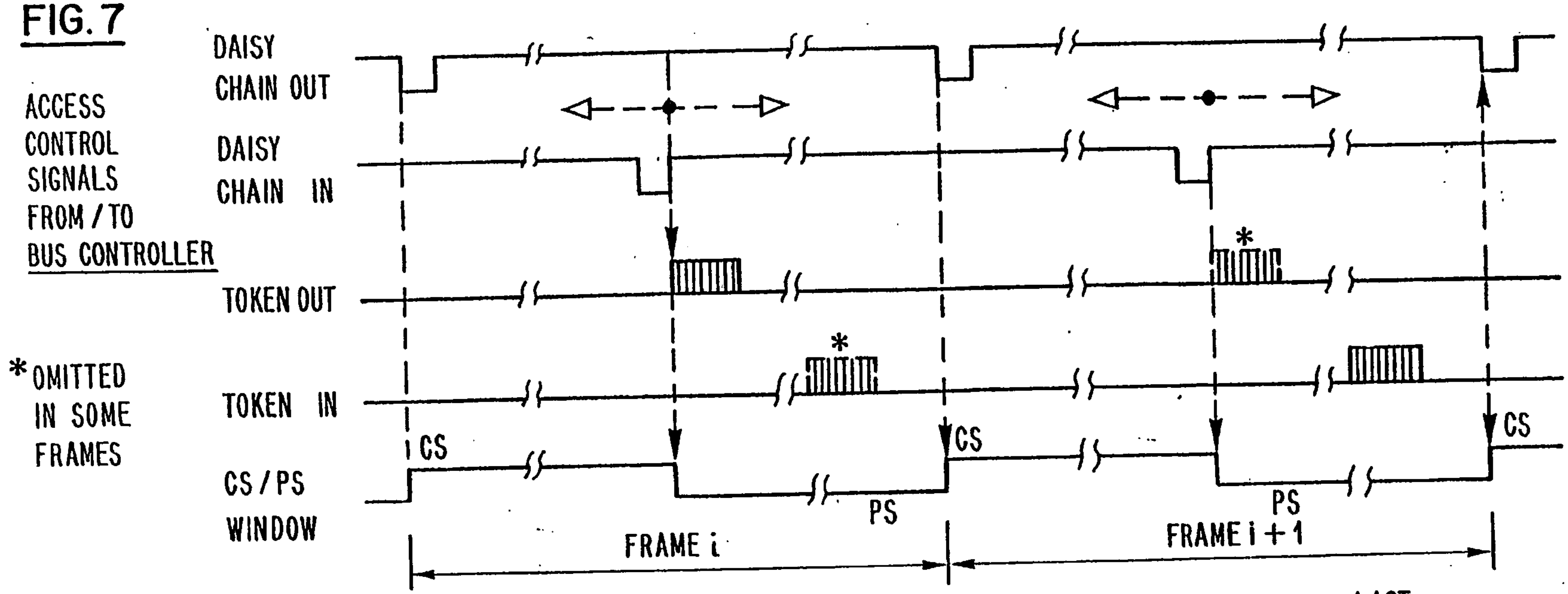
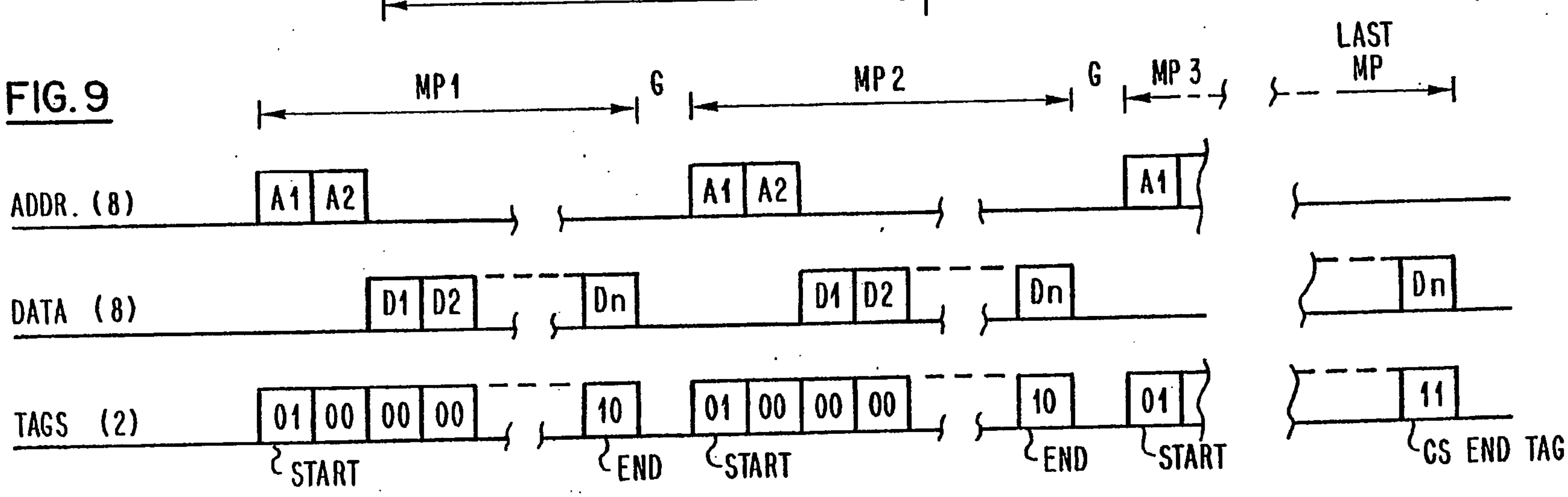

ACCESS
CONTROL
SIGNALS
FROM / TO
BUS CONTROLLER
DAISY CHAIN OUT
DAISY CHAIN IN
TOKEN OUT
TOKEN IN
CS / PS WINDOW
* OMITTED IN SOME FRAMES
CS
PS
FRAME i
FRAME i + 1

FIG. 9


MP1
G
MP2
MP3
LAST MP
ADDR. (8)
DATA (8)
TAGS (2)
A1
A2
D1
D2
Dn
01
00
10
11
START
END
CS END TAG

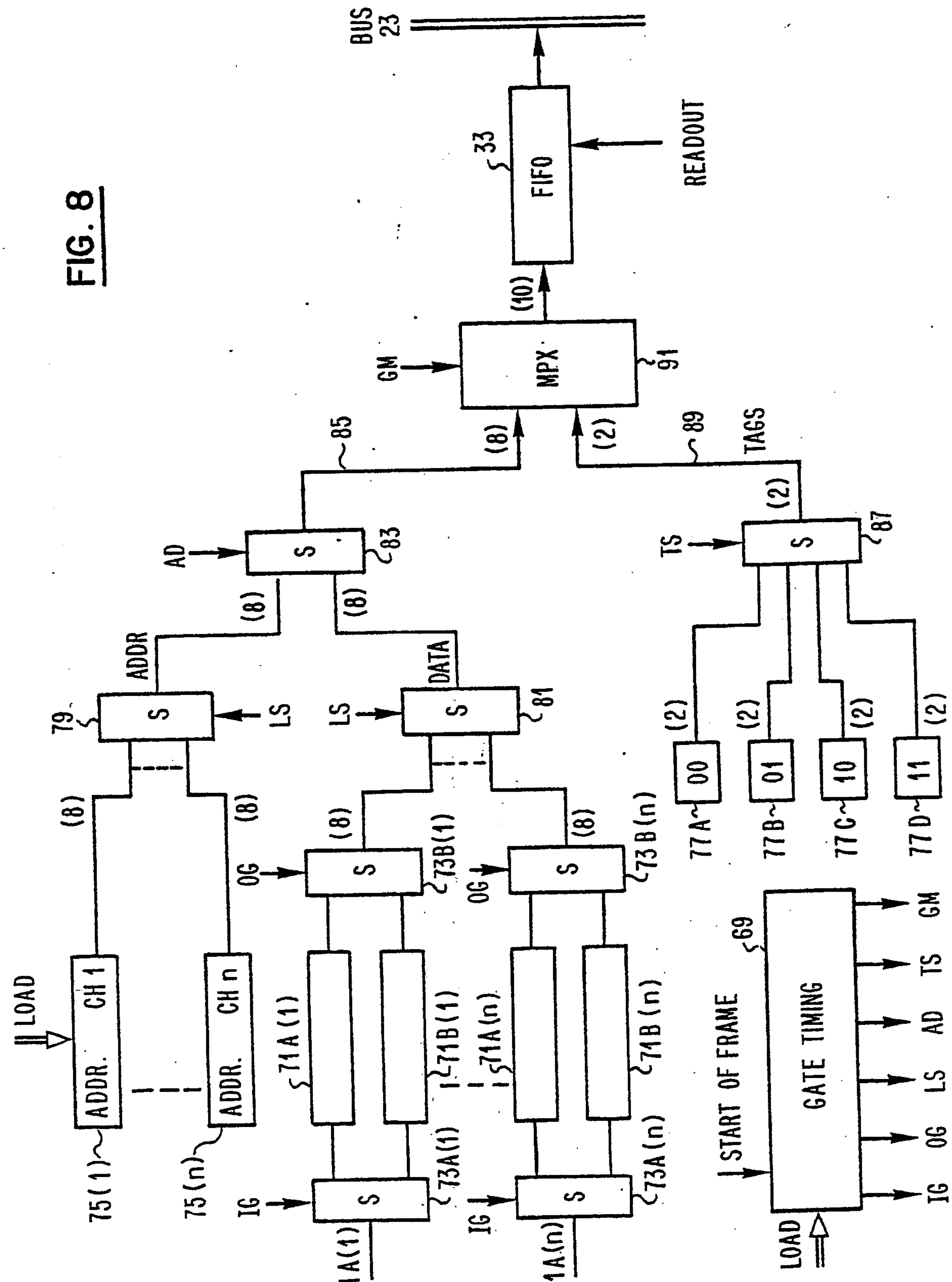

BUS 23
FIFO
33
READOUT
(10)
GM
MPX
91
85
(8)
(2)
89
TAGS
AD
S
83
(8)
(8)
TS
S
87
(2)
ADDR
DATA
79
S
LS
LS
S
81
(2)
(2)
(2)
(2)
00
01
10
11
77 A
77 B
77 C
77 D
(8)
(8)
(8)
(8)
OG
S
73B(1)
OG
S
73 B (n)
LOAD
ADDR.
CH 1
ADDR.
CH n
75(1)
75(n)
71 A (1)
71 B (1)
71 A (n)
71 B (n)
IG
S
73A(1)
IG
S
73A (n)
11 A(1)
11 A(n)
69
START OF FRAME
GATE TIMING
LOAD
GM
TS
AD
LS
OG
IG

FIG. 8

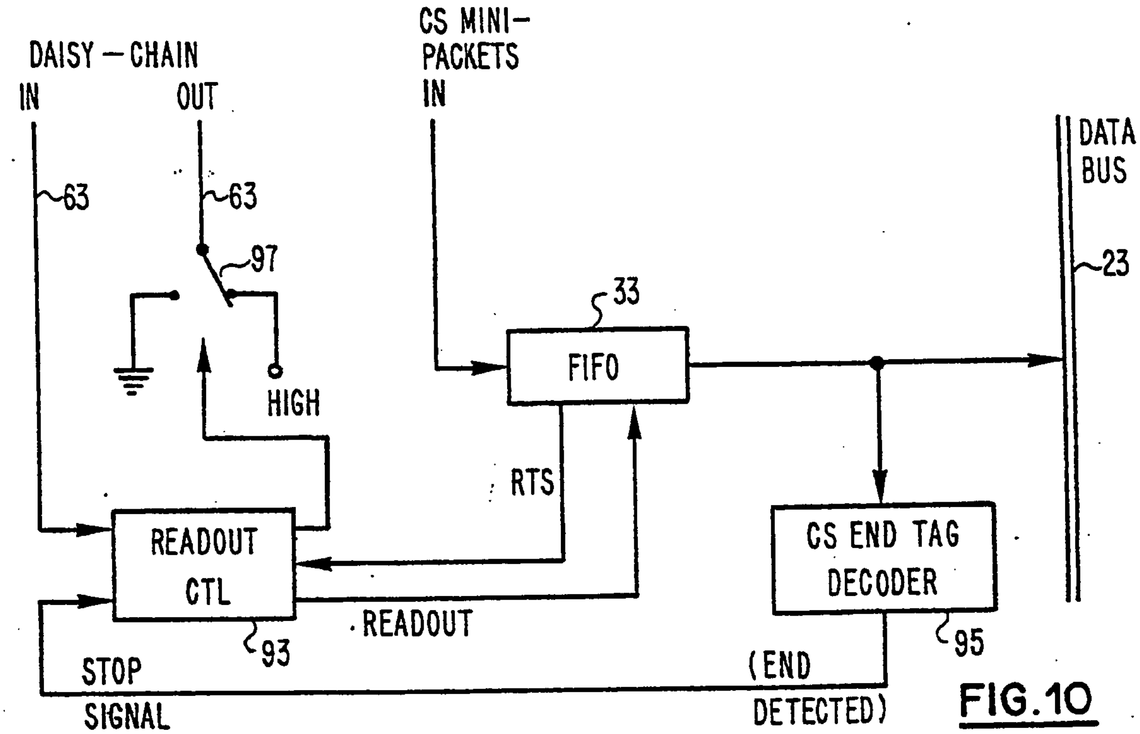

DAISY – CHAIN
IN
OUT
63
63
97
HIGH
CS MINI-
PACKETS
IN
33
FIFO
RTS
READOUT
CTL
93
READOUT
STOP
SIGNAL
CS END TAG
DECODER
95
(END
DETECTED)
DATA
BUS
23

FIG.10

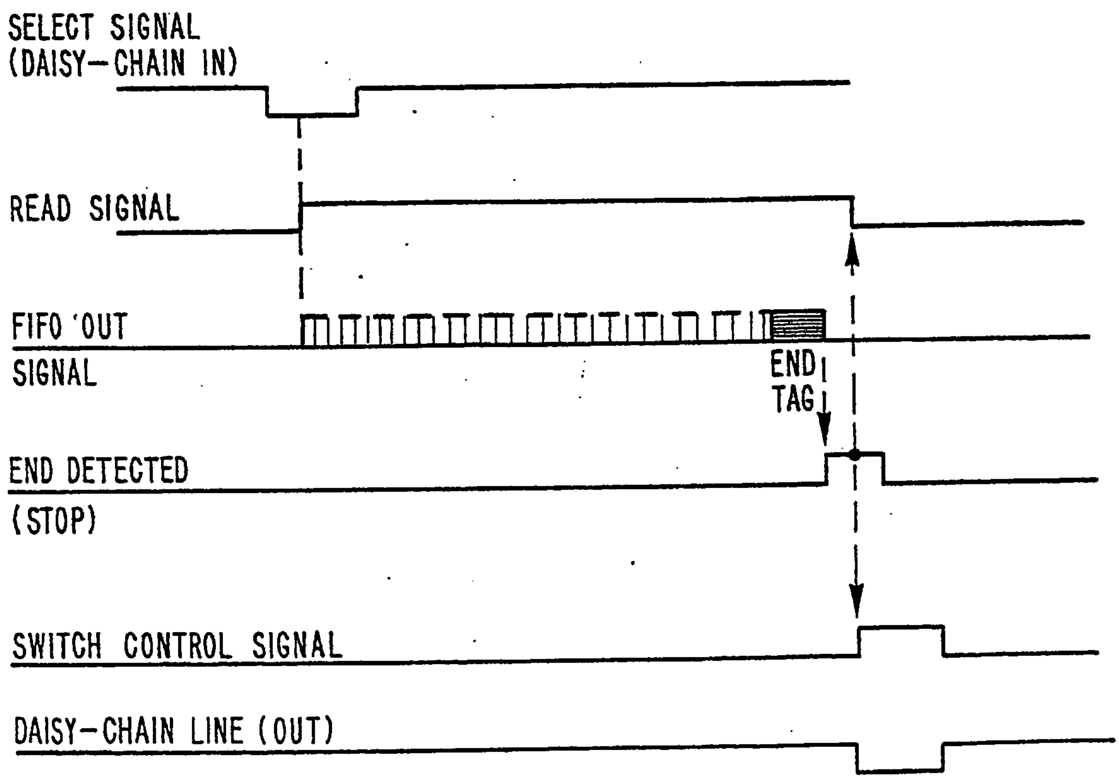

SELECT SIGNAL
(DAISY–CHAIN IN)
READ SIGNAL
FIFO OUT
SIGNAL
END
TAG
END DETECTED
(STOP)
SWITCH CONTROL SIGNAL
DAISY–CHAIN LINE (OUT)

FIG.11

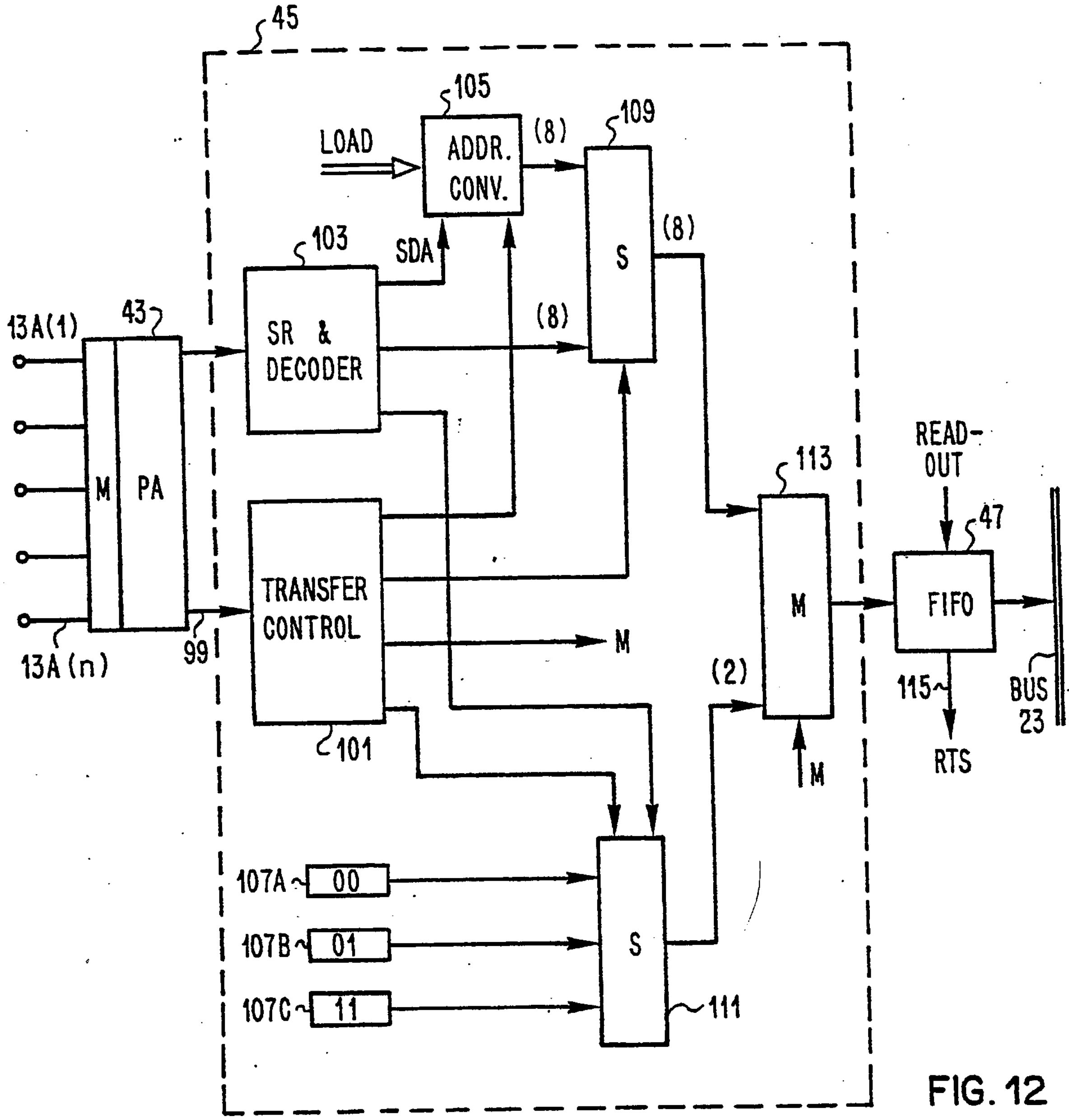

45
105
LOAD
ADDR. CONV.
(8)
109
103
SDA
S
(8)
13A(1)
43
SR & DECODER
(8)
M
PA
READ-OUT
113
47
TRANSFER CONTROL
M
FIFO
13A(n)
99
M
(2)
115
BUS 23
101
RTS
M
107A
00
107B
01
S
107C
11
111

FIG. 12

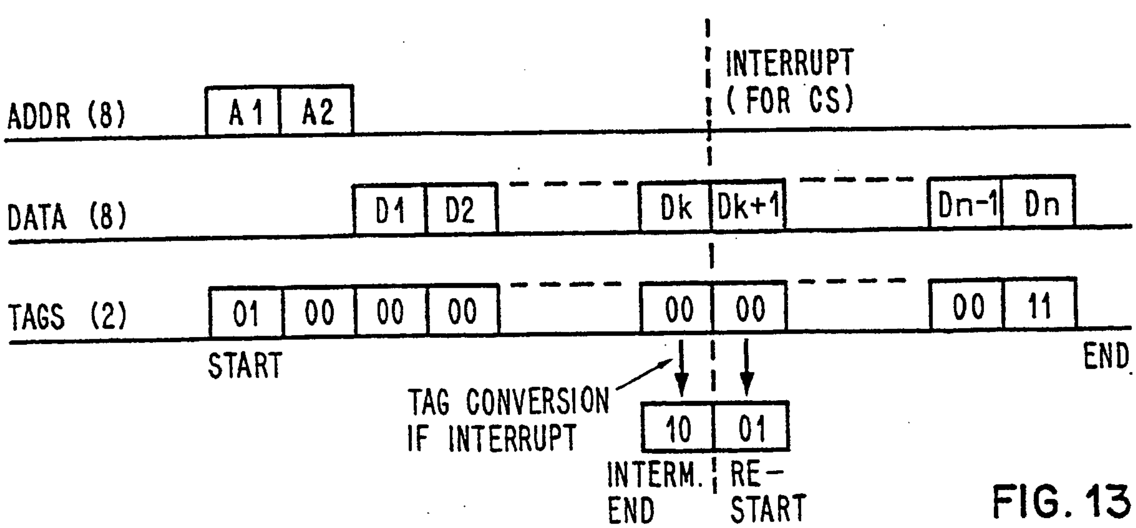

INTERRUPT (FOR CS)
ADDR (8)
A1
A2
DATA (8)
D1
D2
Dk
Dk+1
Dn-1
Dn
TAGS (2)
01
00
00
00
00
00
00
11
START
END
TAG CONVERSION IF INTERRUPT
10
01
INTERM. END
RE-START

FIG. 13

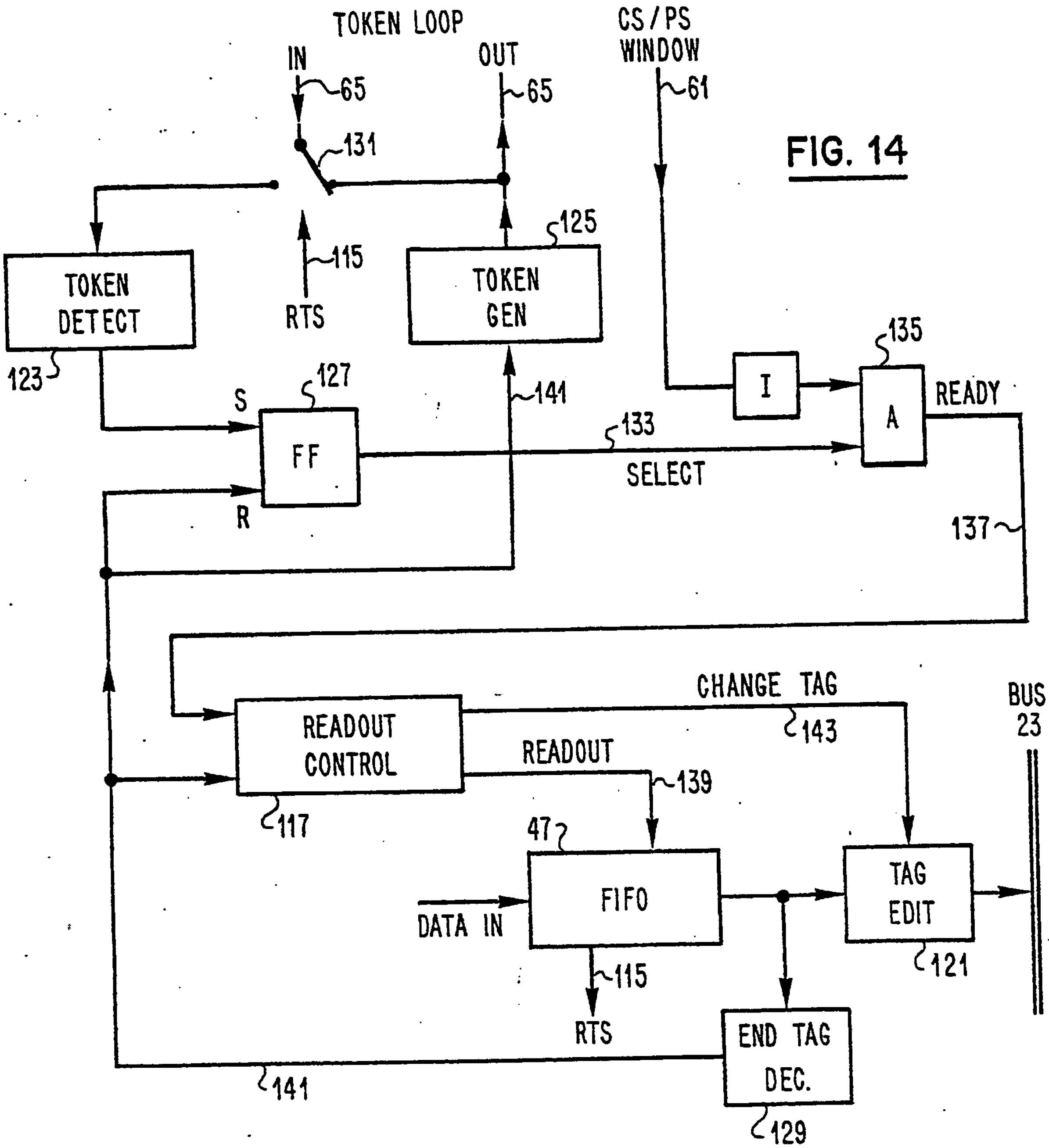
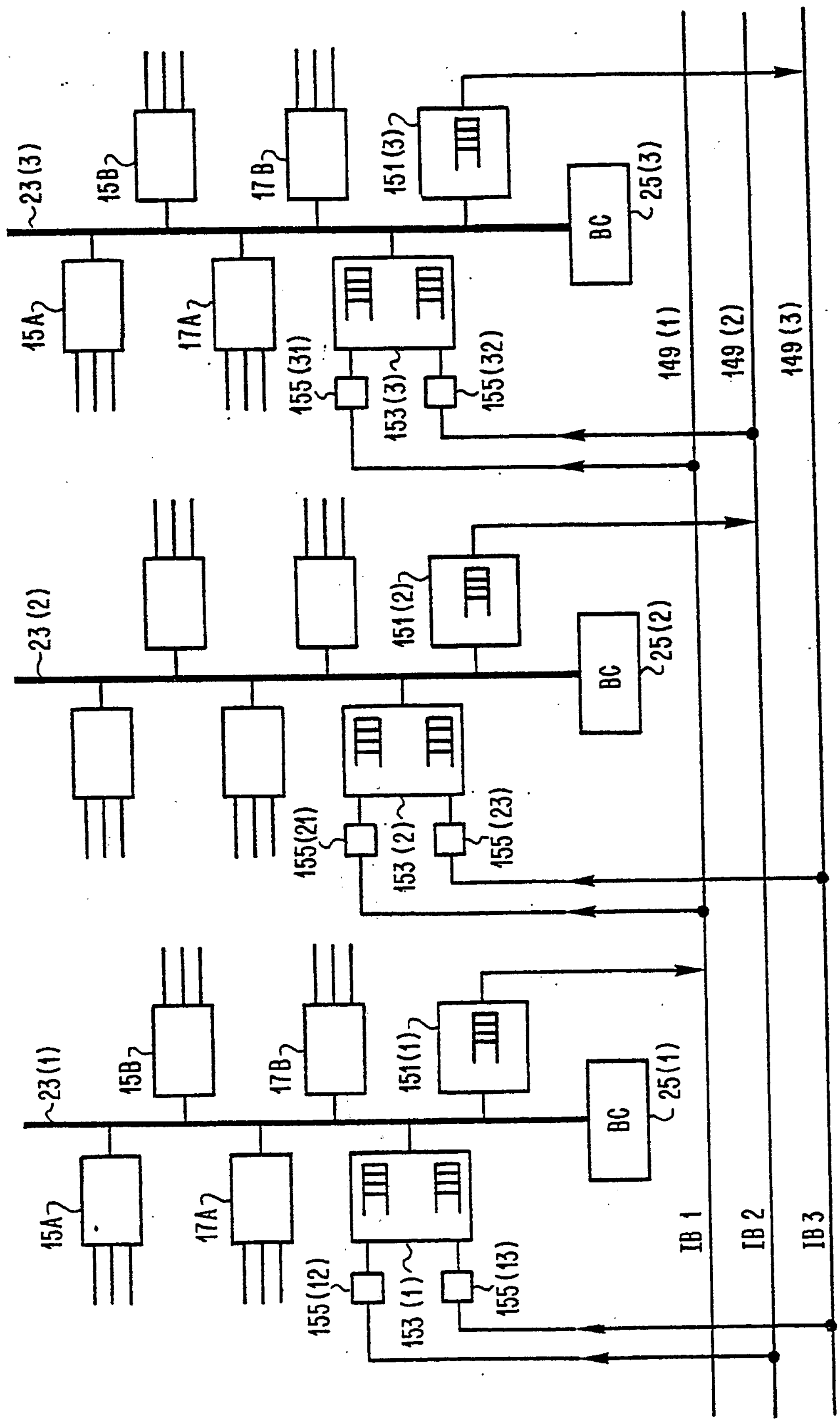

TOKEN LOOP
IN
65
OUT
65
CS/PS
WINDOW
61
131
125
TOKEN
DETECT
115
RTS
TOKEN
GEN
135
123
127
141
I
A
READY
S
133
FF
SELECT
R
137
CHANGE TAG
BUS
23
READOUT
CONTROL
143
READOUT
139
117
47
FIFO
TAG
EDIT
DATA IN
115
121
RTS
END TAG
DEC.
141
129

FIG. 14

FIG. 15


23 (3)
15B
17 B
151 (3)
25 (3)
BC
15A
17A
155 (31)
153 (3)
155 (32)
149 (1)
149 (2)
149 (3)
23 (2)
151 (2)
25 (2)
155 (21)
153 (2)
155 (23)
23 (1)
151 (1)
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155 (13)
IB 1
IB 2
IB 3

European Patent Office

EUROPEAN SEARCH REPORT

Application number

EP 87 10 1194

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.4)
A	COMPUTER NETWORKS AND ISDN SYSTEMS, vol. 10, no. 3/4, October/November 1985, pages 211-219, Washington, D.C., US; E.-H. GOELDNER: "An integrated circuit/packet switching local area network - performance analysis and comparison of strategies" * Page 213, right-hand column, line 25 - page 214, left-hand column, line 23; page 214, right-hand column, lines 5-26; figure 3 *	1-8,11 -13,15	H 04 L 11/20

A	EP-A-0 059 149 (DEVAULT) * Page 1, line 23 - page 2, line 10; page 3, lines 14-39; page 5, lines 19-23; page 5, lines 29-32; page 8, lines 2-6; figures 1A,B,C *	1-3,5, 10,11, 15	**TECHNICAL FIELDS SEARCHED (Int. Cl.4)**
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A,D	EP-A-0 054 077 (I.B.M.) * Page 7, lines 11-22; page 7, line 31 - page 8, line 3; page 8, line 33 - page 9, line 2; page 13, lines 15-24; page 14, lines 14-27 *	1,3,5- 7,10- 12	

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	17-09-1987	DE LA FUENTE DEL AGU

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
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